WEST Search History

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DATE: Sunday, March 06, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L12	L11 and l8	3
☐	L11	(interpacket or intrapacket or (inter adj packet) or (intra adj packet)) adj gap	520
☐	L10	gap near fragmentation near8 packet	0
☐	L9	L8 and l7	14
☐	L8	gap near8 (remove or removal)	10956
☐	L7	20010817	202
☐	L6	gap near8 header near8 (data or payload)near8 (reassembly or assembly)	0
☐	L5	gap near8 header near8 (data or payload)	231
☐	L4	20010817	18
☐	L3	packet near5 (processing or assembling or reassembling or reassembly) near8 gap	25
☐	L2	purpose-built adj router	1
		DB=USPT; PLUR=YES; OP=ADJ	
☐	L1	5638367.pn.	1

END OF SEARCH HISTORY

L2: Entry 1 of 1 File: USPT Oct 19, 2004

DOCUMENT-IDENTIFIER: US 6807594 B1
TITLE: Randomized arbiters for eliminating congestion

Brief Summary Text (6):
To meet the new demands, purpose-built routers were designed. Purpose-built routers are designed and built with components optimized for routing. They not only handled higher line rates and higher network traffic volume, they also added functionality without compromising line rate performance.

Brief Summary Text (7):
A purpose-built router may include a number of input and output ports from which it transmits and receives information packets. A switching fabric may be implemented in the router to carry the packets between the ports. In a high-performance purpose-built router, the switching fabric may transmit a large amount of information. If too much information is simultaneously sent to the switching fabric, or if too much information is destined for a specific destination on the switching fabric, the switching fabric or portions of the switching fabric may become congested.

Detailed Description Text (40):
Although described in the context of a purpose-built router, concepts consistent with the present invention can be implemented in any system that uses multiple arbiters where it is desirable to keep two or more of the arbiters from becoming in-stride with one another. Although the arbiters described herein arbitrate across destinations, an arbiter consistent with the principles of the invention may be used in any system requiring arbitration. For example, data items other than destinations may be randomized.

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L4: Entry 1 of 18 File: PGPB Jul 25, 2002

DOCUMENT-IDENTIFIER: US 20020097733 A1
TITLE: Packet transmitting apparatus

Application Filing Date:
20010524

Summary of Invention Paragraph:
[0018] It is desired that physical bandwidth be usable with 100% effectiveness. To achieve this, it is required that a variable-length packet be output to its destination by stuffing in the packet data without leaving needlessly unallocated bandwidth and without any gaps in terms of time. However, with a complicated scheduler arrangement, as in the prior art, the time for a single scheduling processing cycle is prolonged and packet data cannot be output to the output destination without gaps.

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L4: Entry 3 of 18 File: PGPB Mar 21, 2002

DOCUMENT-IDENTIFIER: US 20020035656 A1
TITLE: Asymmetric data path media access controller

Application Filing Date:
20010801

CLAIMS:

11. The method according to claim 1 wherein the processing step comprises the step of resolving an inter-packet gap.

L4: Entry 5 of 18 File: USPT Dec 10, 2002

DOCUMENT-IDENTIFIER: US 6493120 B1
TITLE: Optical fiber-delay line buffers with void filling

Application Filing Date (1):
19990217

Detailed Description Text (3):
Optical data packet switching or routing is accomplished according to the present invention using a void filling and scheduling procedure that inserts optical packets into gaps or voids created by processing previous optical packets through the output of the optical switch. The present invention provides an improved optical buffer that uses a void filling methodology to increase the performance of a fiber optic switch. The optical buffer of the present invention can accomplish void filling on variable or fixed optical data packets that are either synchronous (i.e., time-slotted) or asynchronous.

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L4: Entry 13 of 18 File: JPAB May 12, 2000

DOCUMENT-IDENTIFIER: JP 2000134218 A
TITLE: PACKET MULTIPLEX PROCESSING SYSTEM

Abstract Text (1):
PROBLEM TO BE SOLVED: To perform high-speed transfer and to enlarge the capacity of a line without being affected by a software processing and without generating a gap on the line relating to a packet multiplex processing system in communication equipment for making packets into ATM cells and transmitting them.

Application Date (1):
19981028

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L4: Entry 18 of 18 File: DWPI Jul 19, 1989

DERWENT-ACC-NO: 1989-208496
DERWENT-WEEK: 198929
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TITLE: Tape packet assembler-disassembler for tape drive system - combines host transmitted records into packets comprising data portion made up of data blocks and trailer portion made of table entries

PF Application Date (1):
19890105

PF Application Date (2):
19890105

PF Application Date (3):
19890105

PF Application Date (5):
19890105

PF Application Date (6):
19890110

PF Application Date (7):
19880108

PF Application Date (8):
19880108

PF Application Date (9):
19890822

Equivalent Abstract Text (1):
Apparatus (7) for assembly and disassembly of packets (43) of data communicated between a host computing environment (1) and a sequentially accessed mass storage device (25) the apparatus comprising: first interface means (8) for coupling to the host computing environment, for receiving host-transmitted records to be written to the mass storage device, and for sending to the host computing environment data and status information read from the mass storage device; characterised by further comprising: tape packet assembly/disassembly means (TPAD) (11 through 22) coupled to the first interface means for assembling into a buffer (13) packets separated by gaps, each packet comprising data portions (14,16,18) (29) and trailer portions (15,17,19) (36) of information corresponding to host-transmitted records, the data portions containing data (31,32) from the host-transmitted records and the trailer portions containing descriptive information (33,37) about the structure of the data portions, including the location of any tape mark that occurred in the host-transmitted record, and for disassembling back into host-transmitted records and associated status indications packets comprising data portions and trailer portions; and second interface means (23) coupled to the TPAD for coupling to the mass storage device (25) for writing packets in the buffer thereto, and for reading

packets therefrom into the buffer.

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L9: Entry 14 of 14 File: USPT Sep 21, 1993

DOCUMENT-IDENTIFIER: US 5247638 A
TITLE: Apparatus for compressing data in a dynamically mapped virtual data storage subsystem

Abstract Text (1):
The use of a dynamically mapped virtual memory system permits the storage of data so that each data record occupies only the physical space required for the data. Furthermore, the data storage subsystem manages the allocation of physical space on the disk drives and does not rely on the file extent defined in the count key data format. Data compaction apparatus is provided to remove the gaps contained in the stream of count key data records received from the host processor. A data compression algorithm is then used to compress the received data into a compressed format for storage on the disk drives. It is the compacted, compressed data that is finally stored on the disk drives. Furthermore, any data record received from the host processor absent data in the user data field therein is simply listed in the virtual memory map as a null field occupying no physical space on the disk drives. The data storage control, through its mapping capability, stores the actual data in the minimum physical space required by overcoming the limitations imposed on large form factor disk drives by the use of count key data format data records. However, the data storage subsystem returns this stored data to the host processor in count key data format through a data record reformatting process once the stored compacted compressed data is staged to the cache memory for access by the host processor. The data storage subsystem is operationally independent of the host processor, yet performs as if it were a standard operationally dependent large form factor disk subsystem.

Application Filing Date (1):
19900618

Brief Summary Text (16):
The use of a dynamically mapped virtual memory system permits the storage of data in the redundancy groups in fixed block format so that the data record occupies only the physical space required for the data. Furthermore, the data storage subsystem manages the allocation of physical space on the disk drives of each redundancy group and does not rely on the file extent defined in the count key data format. A data compression algorithm is used to compress the received data into a compressed format for storage on the disk drives. Data compaction apparatus is provided to remove the gaps contained in the count key data record received from the host processor. It is the compressed, compacted data that is finally stored on the disk drives in the redundancy group. Furthermore, any virtual track received from the host processor absent data in the data records thereof is simply listed in the virtual memory map as a null or unformatted track occupying no physical space on the disk drives in the redundancy groups. The data storage control, through its mapping capability, stores the actual data in the minimum physical space required by overcoming the limitations imposed on large form factor disk drives by the use of count key data format data records. However, the data storage subsystem returns this stored data to the host processor in count key data format through a data record reformatting process once the stored compressed compacted data is staged to the cache memory for access by the host processor. The data storage subsystem is

operationally independent of the host processor, yet performs as if it were a standard operationally dependent large form factor disk drive.

Detailed Description Text (33):
As a data record is received from host processor 11 by channel interface control 202-0, and buffered therein, processor 204-0 deletes all gaps between fields in the received count key data record. The virtual device and virtual cylinder addresses are extracted from the count key data format data record and used to create an entry in the virtual cylinder directory stored in cache memory 113. The data fields of the received data record are forwarded to channel data compression circuit 203-0 for compression and temporary storage in cache memory 113. Thus, all that is stored in the redundancy groups are logical cylinders of compressed data in fixed block architecture format since the headers, gaps and received space in the received count key data are deleted. A further compaction process is the creation of null virtual tracks. Each time host processor 11 creates a new instance of a data file, a predetermined data file extent is reserved by host processor 11. Channel interface control 202-0 and processor 204-0 eliminate the need to reserve this unused memory space by simply creating a series of null entries in the virtual track directory; no data is written to a redundancy group.

Detailed Description Text (62):
As a data record is received from host processor 11 by channel interface control 202-0, and buffered therein, processor 204-0 deletes all gaps between fields in the received count key data record. The virtual device and virtual cylinder and head addresses previously received from the data channel are used to select an entry in the virtual track directory stored in cache memory 113. The data fields of the received data record are then forwarded to channel data compression circuit 203-0 for compression and temporary storage in cache memory 113. Thus, all that is stored in the redundancy groups are logical cylinders of compressed data in fixed block architecture format since the headers, gaps and reserved space in the received count key data are deleted. A further compaction process is the creation of null virtual tracks. Each time host processor 11 creates a new instance of a data file, a predetermined data file extent is reserved by host processor 11. Channel interface control 202-0 and processor 204-0 eliminate the need to reserve this unused memory space by simply creating a series of null entries in the virtual track directory; and no data is written to a redundancy group.

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L12: Entry 3 of 3 File: USPT May 4, 2004

DOCUMENT-IDENTIFIER: US 6731654 B1
TITLE: Communication system overhead channel

Detailed Description Text (21):
The remainder of user payload data 35 can be the Ethernet data that is being transmitted, and is typically passed to the user computer or other device for further processing. Whenever multiple small Ethernet frames are placed within a single user payload data 35, a separate indicator called the Next Frame Flag (NFF) can be used to indicate the condition. The NFF is a byte that may be located in the 12.sup.th byte of the interpacket gap (IGP) of an Ethernet frame. This positioning is preferred as the preferred embodiment Ethernet protocol dictates at least a 12 byte gap be present between Ethernet packets. Accordingly the transmission of such successive Ethernet packets may be accomplished according to the present invention by leaving the required 12 byte interpacket gap and placing a NFF byte in this 12.sup.th, otherwise unused byte, to indicate the multiple Ethernet frame condition. This byte is not shown in FIG. 3, but can be located in the user payload data area 35. The NFF byte preferably indicates an offset at which the next frame begins (i.e., accounts for the variable number of interpacket gap bytes). However, this NFF byte may simply indicate that a second frame is present without indicating any offset information, such as where buffering of the transmitted data is utilized to remove bytes in the interpacket gap in excess of the 12 common to the Ethernet protocol. Of course, it should be appreciated that the placement of the NFF byte may be different from that described above.

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